

Power MOSFET in High-Side Operating Modes, Possible Failure Modes, and Failure Signatures

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Power MOSFETs in high-side application can fail under any one of the following modes of operation:

- (a) High-impedance gate drive
- (b) Electro-static discharge (ESD) exposure
- (c) Electrical over-stressed (EOS) operation

In most cases, failure analysis of the damaged MOSFET reveals a signature that can point towards a possible cause of failure.

(a) High-Impedance Gate Drive

A generic schematic configuration for a high-side driver with inductive load is shown in figure 1. A typical gate drive design based on an application-specific integrated circuit (ASIC) caters to the primary gate charge requirements of the MOSFET, which are on the order of a few tens to hundreds of nanocoulombs. An effort to achieve high efficiency and optimize the integration of the ASIC results in low-current ($< 50 \mu\text{A}$) gate drives (V_2 referenced to power supply ground) with a high output impedance ($> 1 \text{M}\Omega$). This basically satisfies the total gate-charge requirements of the MOSFET. However, to avoid overloading the ASIC, the external gate resistor (R_2) in such a design tends to have a high ohmic value (ranging from tens of ohms to several kilohms). The feedback resistor (R_3) also usually has a high ohmic value (ranging from several kilohms to $1 \text{M}\Omega$). As a result, the source (S) of the power MOSFET (U_1) is virtually floating. The effect is magnified during turn-off and recirculation of the energy stored in the inductor (L_1).

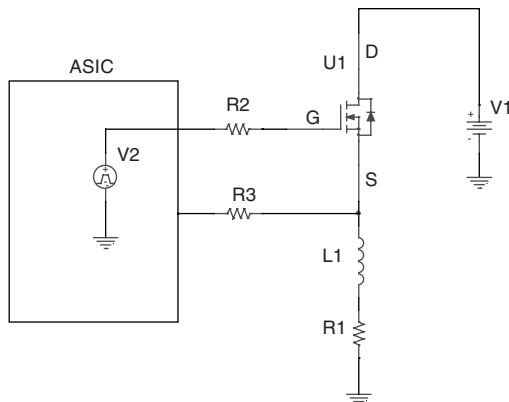


Fig. 1 - Typical High Side Driver

This approach fully satisfies the requirements for steady-state operation, where small amount of current, on the order of a few microamps, is all that is required to maintain the on state. But it can be inadequate for dynamic (transient) turn-on and turn-off operation of MOSFET. In this latter case, the MOSFET switching operation can easily occur in **linear mode**, which is an **unstable** and **non-characterized** area of MOSFET operation (figure 2).

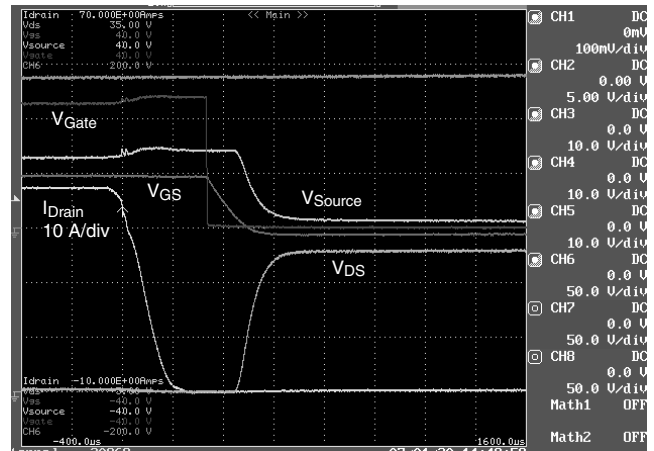


Fig. 2 - Floating Source and Slow Turn-Off

During turn-on and turn-off, switching power losses are likely to dissipate from a very small area of the active die. The resulting failure signature is high-power burn-out, with a random amount of damage located in the active area of the die. Invariably such failure is labeled as **EOS**.

Another subtle failure evidenced during the analysis of the failed MOSFET (with a **virtually floating gate** circuit configuration) is in the gate-source area. A DC parameter test of the gate-source area shows out of spec readings. The failure mode is subtle insofar as the leaky device recovers even during the DC parameter test. This failure mode remains under investigation to obtain a full explanation.

A failure example of a DPAK power MOSFET is shown in the figures 3, 4, and 5.

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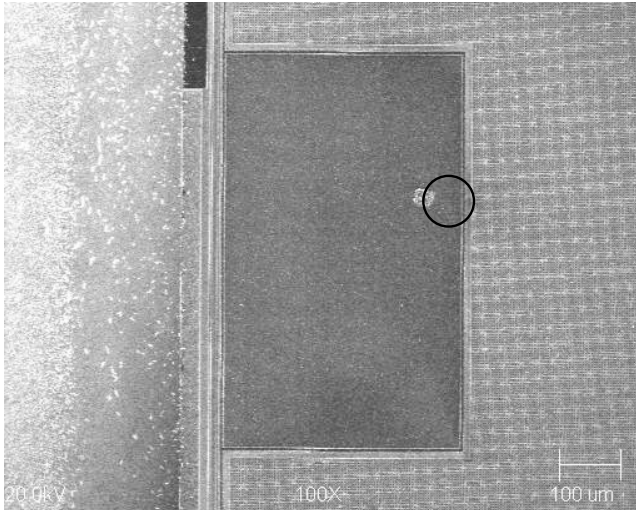


Fig. 3 - EOS dDamage Location

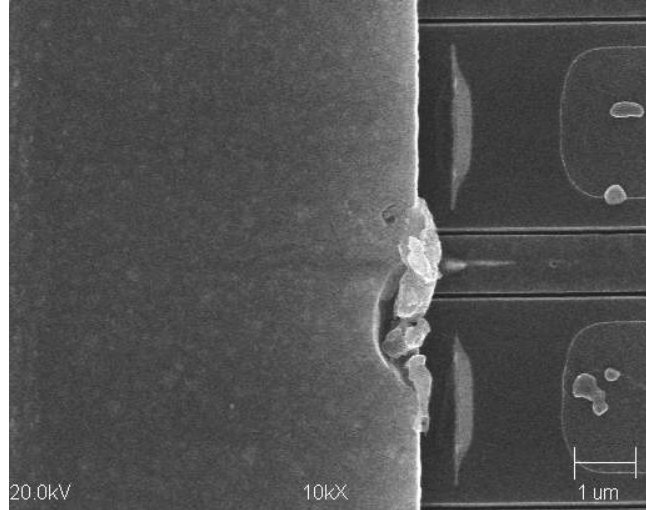


Fig. 5 - Damage on Gate Poly

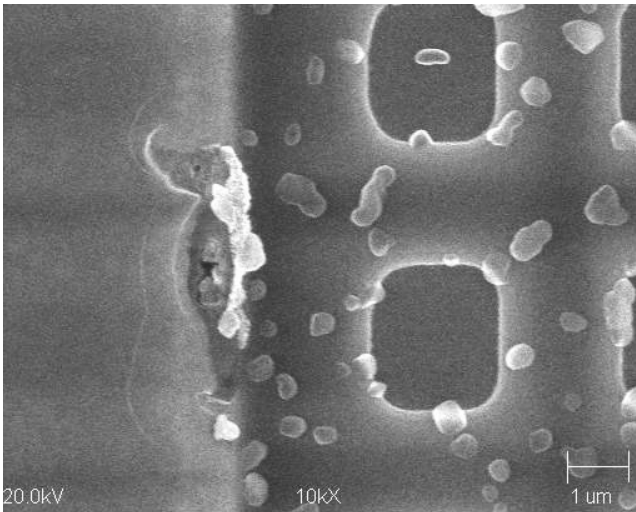


Fig. 4 - Damage on BPSG

(b) Electro-Static Discharge (ESD) Exposures

A second possible scenario arising from a virtually floating gate condition caused by the high impedance of an ASIC driver and/or high gate resistor is increased susceptibility of the gate-source area for damage from ESD or a similar event. In addition to a typical ESD event, high-energy, high-voltage transients of short duration can be generated from energy re-circulation and/or energy interruption from inductive components. With reference to figure 6, these include the low-side load (L1, R1), other parallel connected load (L2, R4), and series feed-in/harness impedance (L3, R5).

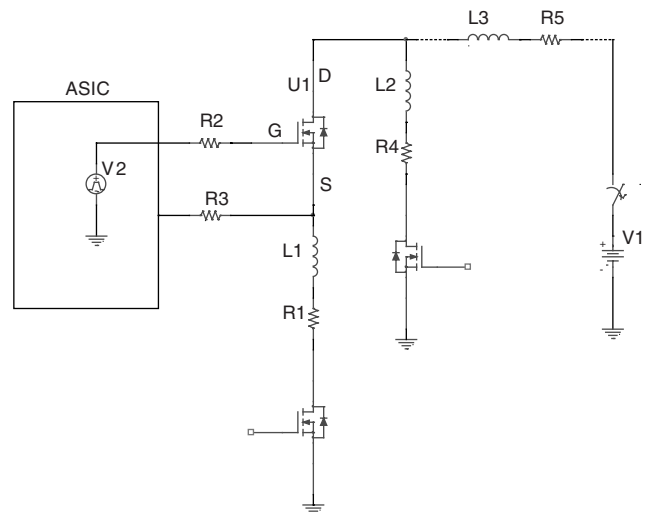


Fig. 6 - L1, L2, L3 Sources of Transients

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Failure signatures are usually located near the gate termination and in the gate-source area. An example of a DPAK power MOSFET failure is shown in figures 7, 8 and 9.

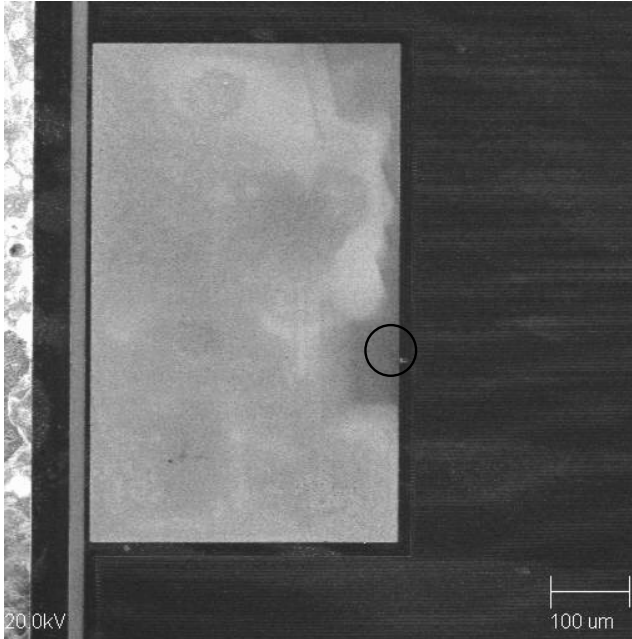


Fig. 7 - ESD Damage near the Gate-Source

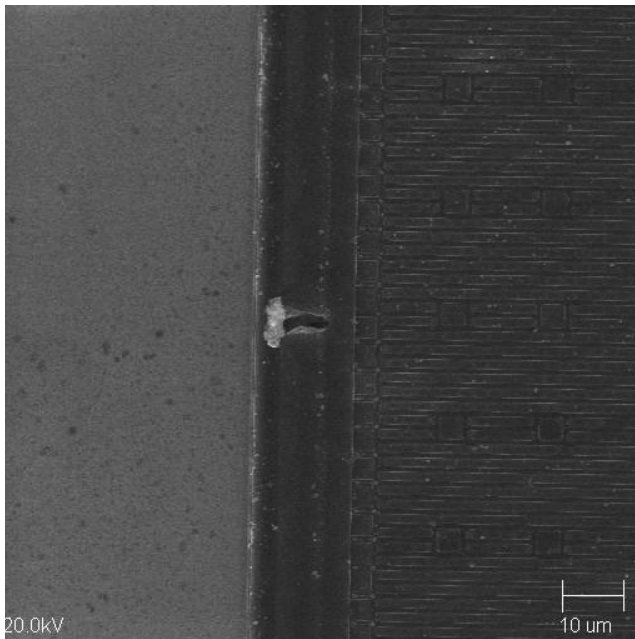


Fig. 8 - ESD on the Gate Termination

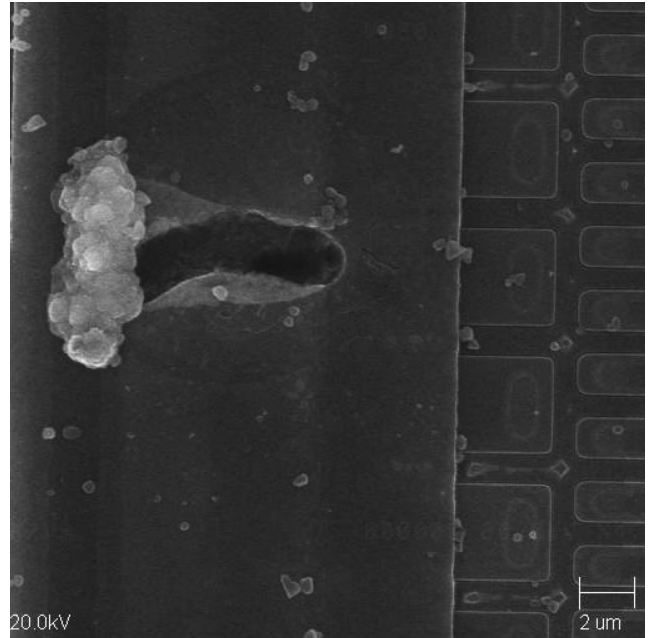


Fig. 9 - Close-up of ESD Damage

(c) Electrical Over Stressed (EOS) Operation

High-energy or high-voltage short-duration transients appearing on the drain-source termination of the MOSFET (figure 6) can result in damage with a variety of signatures.

Transients that are faster than the breakdown time of the body diode may produce punctures anywhere in the active area of the drain-source. Such punctures have the appearance of a pin-hole at the damage site. They may be attributed to an ESD event or an ESD-like event arising from other circuit components or parasitics.

Where energy/voltage values are not too high but of a sufficient duration to break down the body diode, **avalanche** results. Avalanche results in extensive damage and in fact destroys the evidence that failure analysis would need to determine the root cause. These are true EOS events.

EOS can also result from a mismatch of thermal management and continuous power dissipation in the device, even when the device is fully turned on. When heat-sinking is inadequate, heat can build up in the junction during continuous operation. Eventually a thermal runaway occurs. The device is completely destroyed and also classified as an EOS.

D²PAK example: figures 10 to 12 are failure signatures for a D²PAK power MOSFET.

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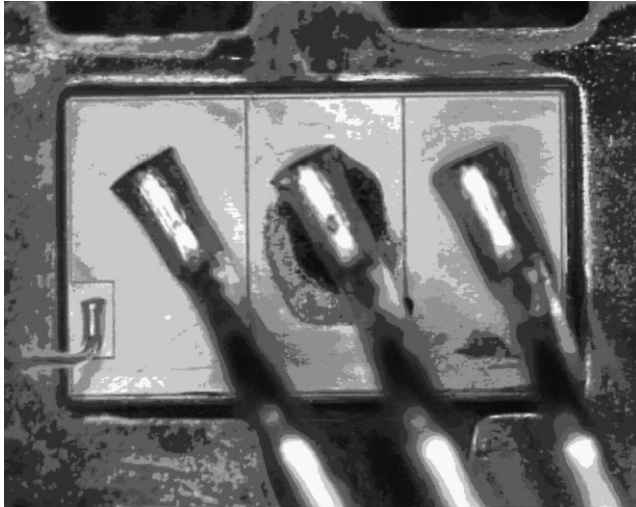


Fig. 10 - High Power EOS (after Decapsulation)

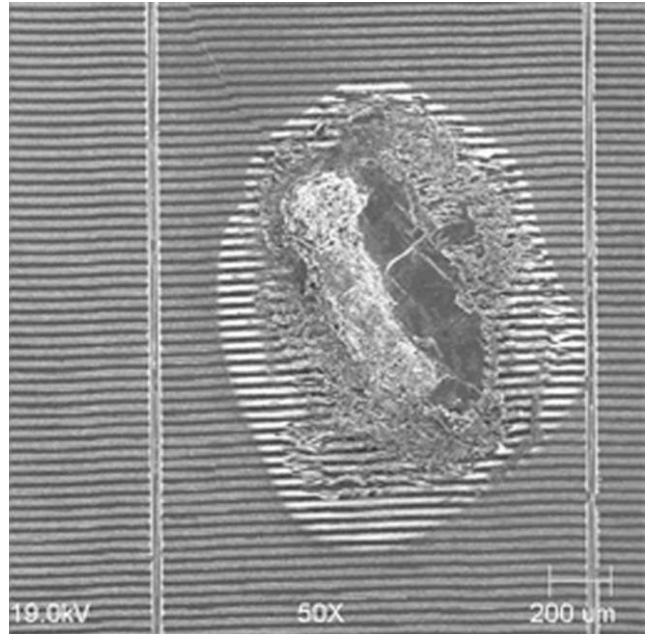


Fig. 12 - EOS Damage at 50 x Magnification

SO-8 dual example: figures 13 to 15 are another example of a dual SO-8 power MOSFET failure identified as EOS

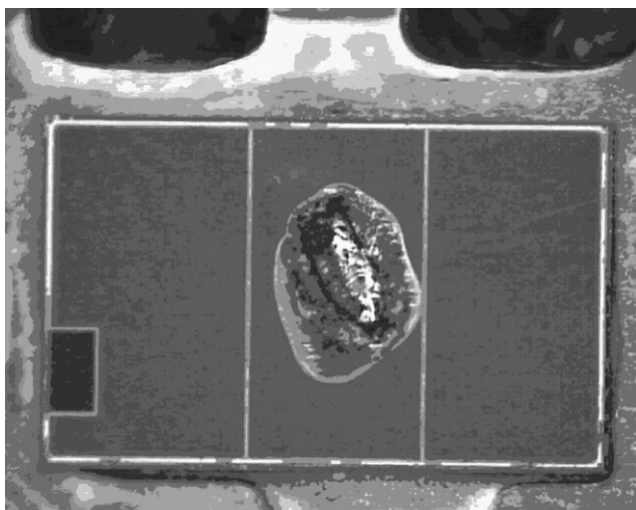


Fig. 11 - EOS Signature after Removing Top Metal Layer

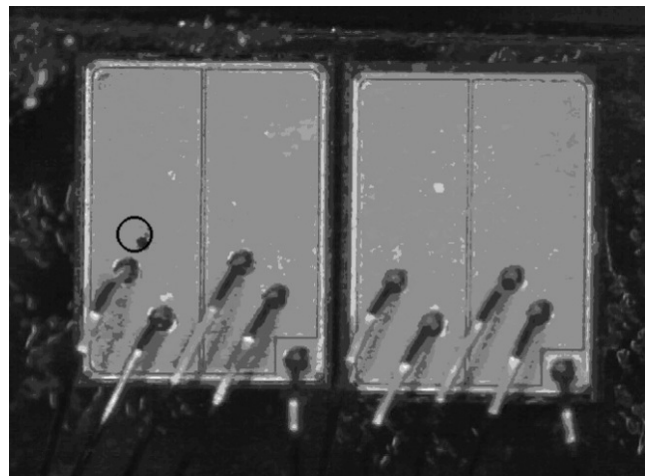


Fig. 13 - Failure near Bond Wire

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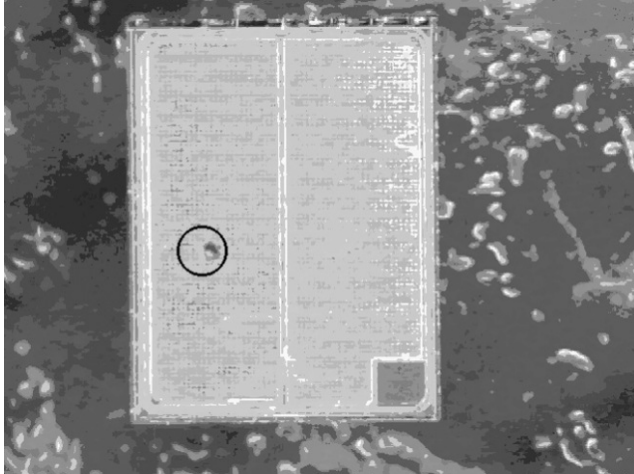


Fig. 14 - EOS in Active Region

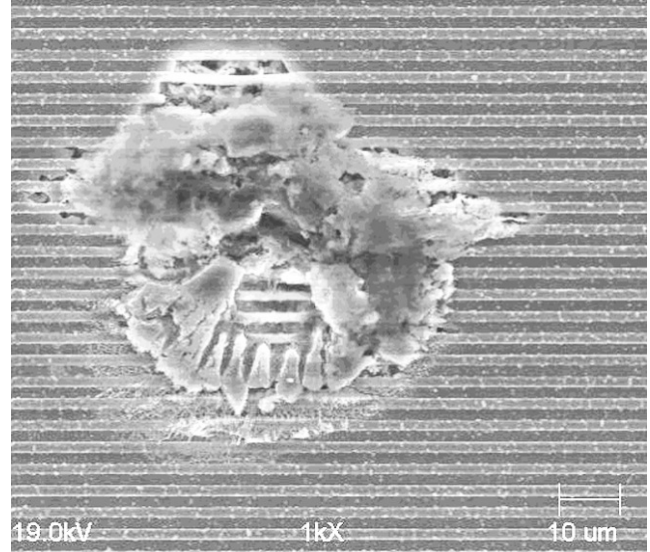


Fig. 15 - Close-up of EOS Damage

SUMMARY

Power MOSFET failures in high-side applications can often be attributed to a high-impedance gate drive creating a virtual floating gate, which in turn increases the susceptibility of the MOSFET to failure during system-generated ESD and EOS scenarios.

Failure signatures are associated with:

- EOS-type damaged inter layer die-electric (ILD) film between the source metal and gate polysilicon
- ESD-type damage near the gate termination and gate-source area
- High energy/prolonged operation of the EOS-damaged drain-source active area